WHAT IS CLAIMED IS:

1. A method of testing a memory instance, comprising:

scanning test information into a test and repair wrapper integrated with said memory instance;

providing a strobe control signal to said test and repair wrapper for signaling commencement of testing operations with respect to said memory instance;

generating, by said test and repair wrapper, at least one of an address signal, a data signal and a command signal based on said scanned test information; and

executing at least one test with respect to said memory instance responsive to said address, data and command signals generated in said test and repair wrapper.

2. The method of testing a memory instance as set forth in claim 1, wherein said step of scanning test information is effectuated by a built-in self-test and repair (BISTR) processor associated with said memory instance.

3. The method of testing a memory instance as set forth in claim 1, wherein said strobe control signal is provided to said test and repair wrapper by a built-in self-test and repair (BISTR) processor associated with said memory instance.

4. The method of testing a memory instance as set forth in claim 1, wherein said at least one test is executed at speed using a memory clock operable with said memory instance.

5. The method of testing a memory instance as set forth in claim 4, wherein said at least one test comprises a single cycle write operation.

6. The method of testing a memory instance as set forth in claim 4, wherein said at least one test comprises a single cycle read operation.

7. The method of testing a memory instance as set forth in claim 4, wherein said at least one test comprises a single cycle, simultaneous read and write operation.

8. The method of testing a memory instance as set forth in claim 4, wherein said at least one test comprises a back-to-back write operation.

9. The method of testing a memory instance as set forth in claim 8, wherein said back-to-back write operation is followed by a read operation.

10. The method of testing a memory instance as set forth in claim 4, wherein said at least one test comprises a back-to-back read operation.

11. The method of testing a memory instance as set forth in claim 10, wherein said back-to-back read operation is followed by a write operation.

12. The method of testing a memory instance as set forth in claim 1, wherein said test and repair wrapper is generated by a memory compiler used for compiling said memory instance.

13. The method of testing a memory instance as set forth in claim 12, wherein said memory compiler is operable to compile multiple memory instances, each having a different aspect ratio.

14. The method of testing a memory instance as set forth in claim 12, wherein said memory compiler is operable to compile a memory instance selected from the group consisting of a static random access memory (SRAM) instance, an electrically programmable read-only memory (EPROM) instance, a dynamic random access memory (DRAM) instance, a Flash memory instance, and a register file (RF) memory instance.

15. The method of testing a memory instance as set forth in claim 12, wherein said memory compiler is operable to compile multiple memory instances, each having a test and repair wrapper integrated therewith.

16. An apparatus for testing a memory instance, comprising:

a built-in self-test and repair (BISTR) processor associated with said memory instance for scanning test information into a test and repair wrapper integrated with said memory instance, wherein said test and repair wrapper is operable to commence testing operations with respect to said memory instance responsive to a strobe control signal provided by said BISTR processor; and

logic circuitry associated with said test and repair wrapper for generating at least one of an address signal, a data signal and a command signal based on said scanned test information, wherein at least one test may be executed with respect to said memory instance responsive to said address, data and command signals.

17. The apparatus for testing a memory instance as set forth in claim 16, wherein said at least one test is executed at speed using a memory clock operable with said memory instance.

18. The apparatus for testing a memory instance as set forth in claim 16, wherein said at least one test comprises a single cycle write operation.

19. The apparatus for testing a memory instance as set forth in claim 16, wherein said at least one test comprises a single cycle read operation.

20. The apparatus for testing a memory instance as set forth in claim 16, wherein said at least one test comprises a single cycle, simultaneous read and write operation.

21. The apparatus for testing a memory instance as set forth in claim 16, wherein said at least one test comprises a back-to-back write operation.

22. The apparatus for testing a memory instance as set forth in claim 21, wherein said back-to-back write operation is followed by a read operation.

23. The apparatus for testing a memory instance as set forth in claim 16, wherein said at least one test comprises a back-to-back read operation.

24. The apparatus for testing a memory instance as set forth in claim 23, wherein said back-to-back read operation is followed by a write operation.

25. A memory compiler for compiling at least one self-Test and repair (STAR) memory instance, comprising:

a code portion for generating a built-in self-test and repair (BISTR) processor associated with said at least one STAR memory instance; and

a code portion for generating a test and repair wrapper operable to be integrated with said at least one STAR memory instance, wherein said test and repair wrapper functions, responsive to test information scanned in by said BISTR processor, to generate address, data and command signals for effectuating at least one test with respect to said STAR memory instance.

26. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said at least one test is operable to be executed at speed using a memory clock operable with said STAR memory instance.

27. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said at least one test comprises a single cycle write operation.

28. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said at least one test comprises a single cycle read operation.

29. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said at least one test comprises a single cycle, simultaneous read and write operation.

30. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said at least one test comprises a back-to-back write operation.

31. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said back-to-back write operation is operable to be followed by a read operation.

32. The memory compiler for compiling at least one STAR memory instance as set forth in claim 25, wherein said at least one test comprises a back-to-back read operation.

33. The memory compiler for compiling at least one STAR memory instance as set forth in claim 32, wherein said back-to-back read operation is operable to be followed by a write operation.